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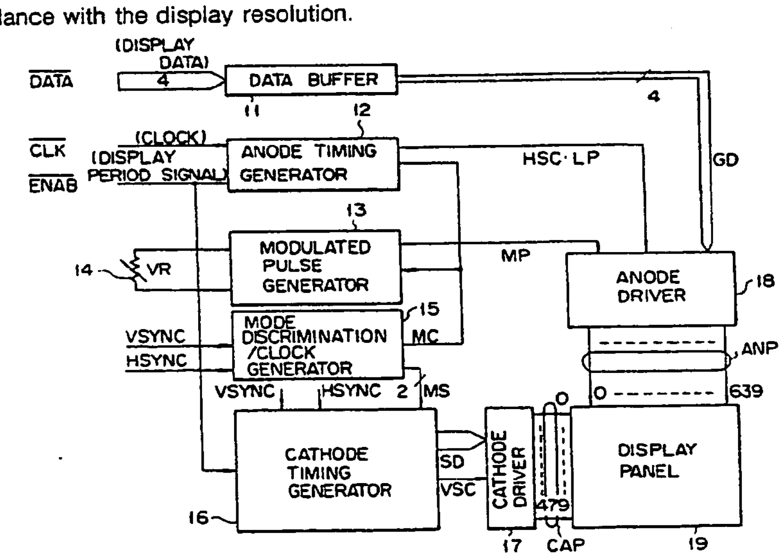
(54) Plasma display control system.

(57) A plasma display includes a mode discrimination/clock generator (15). A CRT display controller (1) generates vertical and horizontal sync signals having polarities. The mode discrimination/clock generator (15) discriminates the polarities of the vertical and horizontal sync signals to determine a display resolution. Anode and cathode timing generators (12, 16) generate display timing signals in accordance with the display resolution.



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Plasma display control system

The present invention relates to a plasma display control system for driving a plasma display at the display timing of a CRT display.

In general, in display control of a CRT display, a vertical blanking period (0.008 sec to 0.0013 sec) including a vertical sync signal and front and back porches at the beginning and end of this signal is necessary. On the other hand, in display control of a plasma display, the above-mentioned long vertical blanking period is not required. Therefore, the plasma display and the CRT display have a different display timing for display drive control. Therefore, in a lap-top type personal computer which has a plasma display and a CRT display which can be connected as an external device, a display timing circuit is required to control the plasma display and the display timing circuit must also drive the CRT display. Furthermore, a switching circuit for switching the display timings is also required, resulting in a complex arrangement.

In the CRT display, since a front porch (1.2 µsec) and a back porch (3.81 µsec) must be large to provide a display margin, so that if a frame is offset slightly (by several characters) in a horizontal or vertical direction, the entire frame can still be displayed.

On the other hand, since the plasma display has no display margin, when the identical frame is displayed using the same display timing as the CRT display, the frame will be partially omitted and not displayed on the plasma display.

It is an object of the present invention to provide a plasma display control system which can display-control a plasma display using the same display timing as for the CRT display.

It is another object of the present invention to provide a plasma display control system wherein when an identical frame is displayed at the same display timing as a CRT display, even if the frame is offset by several characters in the horizontal or vertical direction on the CRT display, the entire frame can be accurately displayed on the plasma display regardless of the resolution selected.

In order to achieve the above objects, according to the present invention, a plasma display control system comprises a plasma display and allows for the optional connection of a CRT display regardless of which of a plurality of resolutions is selected. A CRT controller outputs vertical and horizontal sync signals and data to be displayed on the CRT display and the plasma display. Display resolution discriminating means discriminates between the polarities of the vertical and horizontal sync signals and determines therefrom the display resolution. A display timing generating means generates a display timing signal in accordance with the display resolution and drive means drives the plasma display responsive to the display timing signal.

According to the present invention, in a personal computer which comprises a plasma display and allows for a CRT display to be connected thereto, an arrangement of the display control can be simplified, to produce economical advantages. Display software (e.g., BIOS and application software) created for the CRT display can be used for the plasma display without any modifications.

Other objects and features of the present invention will be apparent from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram showing the overall arrangement of a plasma display control system;

Fig. 2 is a block diagram showing an internal arrangement of the plasma display shown in Fig. 1;

Figs. 3A through 3J are timing charts showing various signals supplied to the plasma display shown in Fig. 2;

Figs. 4A through 4R are timing charts showing signal states of respective portions in a plasma display having a display resolution of 640 × 480 dots;

Figs. 5A through 5O are timing charts showing signal states of respective portions of a plasma display having a display resolution of 640 × 400 dots (or 640 × 350 dots);

Fig. 6 is a table showing the relationship between polarities of a vertical sync signal (VSYNC) and a horizontal sync signal (HSYNC) supplied to a mode discrimination/clock generator 15 shown in Fig. 2, and display resolutions (640 × 480 dots/640 × 400 dots/640 × 350 dots) discriminated on the basis of the polarity states, and signal durations of the respective portions shown in Figs. 3A through 3J at the corresponding display resolutions;

Figs. 7A through 7C are views showing display/non-display areas at the corresponding display resolutions;

Fig. 8 is a detailed block diagram showing an internal arrangement of the cathode timing generator shown in Fig. 2;

Figs. 9A through 9G are timing charts showing the timing of signals supplied to respective portions of the cathode timing generator shown in Fig. 8;

Fig. 10 is a detailed block diagram showing another embodiment of the cathode timing generator shown in Fig. 2;

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Figs. 11A through 11F are timing charts showing the timing of signals at respective portions of the cathode timing generator in the block diagram shown in Fig. 10;

Figs. 12A through 12D are views for explaining a display position offset when no display period signal (ENAB) is used in the embodiment shown in Fig. 8;

Figs. 13A through 13F are views showing differences in display position offset states between arrangements with and without using the display period signal (ENAB);

Fig. 14 is a block diagram of a circuit for generating a vertical shift clock signal (VSC) having a smaller pulse width to that of the cathode timing generator to set a display area at a central portion of a plasma display when a selected display resolution is below a maximum display resolution of the plasma display; and

Figs. 15 and 16 are block diagrams of circuits for discriminating polarities of horizontal and vertical sync signals, respectively.

Fig. 1 is a block diagram showing the overall arrangement of a display controller according to the present invention.

In Fig. 1, a plasma display controller 6 according to the present invention has a CRT controller 1 which outputs various display control signals for controlling display of a cathode ray tube (CRT) 5 and a plasma display (PDP) 4. More specifically, the CRT controller 1 outputs a vertical sync signal (VSYNC), a horizontal sync signal (HSYNC), and an enable signal ($\overline{ENAB}$) indicating the output timing of display data $\overline{DATA}$, which are generated according to display timings of the CRT 5, to the CRT 5 and the PDP 4 through driver 3. The CRT controller 1 described above may adopt the PVGA1 available from Paradise, U.S.A. The polarities (negative/positive) of the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC) output from the CRT controller 1 are changed in accordance with display resolutions (for example 640 × 480 dots, 640 × 400 dots, and 640 × 350 dots shown in Figs. 7A through 7C in this embodiment) of the CRT 5 and the PDP 4, as shown in Fig. 6. A clock module 2 supplies a clock signal $\overline{CLK}$ to the PDP 4 through the driver 3.

Fig. 2 is a block diagram showing the internal arrangement of the PDP 4.

In Fig. 2, a data buffer 11 successively receives the display data DATA (4 bits/pixel: 16 gradation levels) supplied from the CRT controller 1, and outputs it as gradation data (GD). An anode timing generator 12 receives a clock ($\overline{CLK}$), a display period signal ($\overline{ENAB}$), and a clock (MC) from a mode discrimination/clock generator 15, and outputs a horizontal shift clock (HSC) shown in Fig. 4P, a latch pulse (LP) shown in Fig. 4Q, and the like. A modulated pulse generator 13 generates a modulated pulse (MP) on the basis of the clock (MC) generated by the mode discrimination/clock generator 15. A variable resistor 14 performs uniform luminance adjustment for the entire gradation by changing the pulse width of the modulated pulse (MP) generated from the modulated pulse generator 13. The mode discrimination/clock generator 15 discriminates the display resolution of a display screen on the basis of a negative/positive polarity of the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC), outputs a mode switching signal (MS), and also generates various internal clocks (MC). A cathode timing generator 16 receives the display period signal ($\overline{ENAB}$), the vertical sync signal (VSYNC), the horizontal sync signal (HSYNC), the mode switching signal (MS: 2 bits) generated from the mode discrimination/clock generator 15, and generates signals such as scanning data (SD), a vertical shift clock (VSC), and the like for driving the cathode electrodes. A cathode driver 17 receives the scanning data (SD) and the vertical shift clock (VSC) generated from the cathode timing generator 16, and outputs cathode pulses (CAP0 through CAP479) for driving the cathode electrodes. An anode driver 18 receives the gradation data (GD) from the data buffer 11, and the horizontal shift clock (HSC) and the latch pulse (LP) from the anode timing generator 12, fetches the gradation data (GD) in its internal shift register in response to the horizontal shift clock (HSC), latches data of 640 pixels in its internal latch circuit in response to the latch pulse (LP), and performs pulse-width control in accordance with the modulated pulse (MP) to output anode pulses (ANP0 through ANP639) each having a pulse width corresponding to gradation of pixel data. A display panel 19 receives at the cathode electrodes the cathode pulses (CAP0 through CAP479) output from the cathode driver 17, also receives at the anode electrodes the anode pulses (ANP0 through ANP639), and outputs display data at a maximum display resolution of 640 × 480 dots (16 gradation levels).

Figs. 3A through 3J are timing charts showing various timings of signals supplied to the PDP 4 having the internal arrangement shown in Fig. 2. In the timing charts shown in Figs. 3A through 3J, reference symbol t1 denotes a one-frame period; t2, a vertical sync signal (VSYNC) period; t3, a vertical back porch (see VBP in Fig. 13B) included in a vertical blanking period; t7, a one-line display period; t5, a vertical front porch (see VFP in Fig. 13B) included in the vertical blanking period; t8, a vertical sync signal (HSYNC) period; t9, a horizontal back porch (see HBP in Fig. 13B); t10, an effective display data width corresponding to the

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duration of the display period signal ($\overline{ENAB}$); and t11, a horizontal front porch (see HFP in Fig. 13B). Fig. 6 shows detailed durations of these signals.

Figs. 4A through 4R are timing charts showing signal states of respective portions in the PDP 4 having a display resolution of 640 × 480 dots shown in Fig. 7A. Furthermore, Figs. 5A through 5O are timing charts showing signal states of respective portions in the PDP 4 having a display resolution of 640 × 400 dots shown in Fig. 7B or 640 × 350 dots shown in Fig. 7C. In this embodiment, the vertical shift clock (VSC) having a shorter interval than a display area is generated for upper and lower non-display areas corresponding to 40 lines of the display screen.

Fig. 14 shows a circuit for generating the signal VSC having a pulse width smaller than that of a display area for a non-display area of 40 lines. A pulse generator 43 generates the signal VSC having a smaller pulse width than the display area. The signal VSC from the generator 43 and the signal HSYNC from the CRT controller 1 are input to a selector 41. A count output from counter 47 is supplied to a selection terminal of the selector 41 as a selection signal. A value for counting 40 lines is set in the counter 47 as an initial value. The selector 41 first selects the signal VSC from the generator 43. Thereafter, when the counter 47 counts the value for 40 lines, the selector 41 outputs the signal HSYNC. With this arrangement, the signal VSC having a smaller pulse width than that for the display area can be generated for the non-display area of 40 lines.

Fig. 6 is a table showing the relationship between polarities of the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC), and display resolutions (640 × 480 dots/640 × 400 dots/640 × 350 dots) discriminated on the basis the polarity states by the mode discrimination/clock generator 15, and signal durations of the respective portions shown in Figs. 3A through 3J at the corresponding display resolutions. Note that values in parentheses indicate those at the resolution of 640 × 350 dots. These values are constants set in the CRT controller 1, and are pre-stored in a BIOS ROM (not shown).

The mode discrimination/clock generator 15 has circuits shown in Figs. 15 and 16. Fig. 15 shows a circuit for discriminating the polarity of the signal VSYNC. The circuit shown in Fig. 15 comprises a counter 51 and a comparator 53. Fig. 16 shows a circuit for discriminating the polarity of the signal HSYNC. The circuit shown in Fig. 16 comprises a counter 55 and a comparator 57. The counter 51 counts the number of pulses of the signal VSYNC when the signal HSYNC is at low level, and counts that of the signals VSYNC when the signal HSYNC is at high level, and both the counts are compared by the comparator 53, thereby discriminating the polarity of the signal VSYNC. Similarly, the number of the signals CLK when the signal HSYNC is at low level and that of the signals CLK when the HSYNC is at high level are respectively counted by the counter 55, and the count values are compared by the comparator 57, thereby discriminating the polarity of the signal HSYNC.

Figs. 7A through 7C show the relationship of the display/nondisplay areas at the corresponding display resolutions (640 × 480 dots/640 × 400 dots/640 × 350 dots). Fig. 7A corresponds to the resolution of 640 × 480 dots, Fig. 7B corresponds to the resolution of 640 × 400 dots, and Fig. 7C corresponds to the resolution of 640 × 350 dots. When the display resolution is lower than the physically maximum resolution on the display panel 19, such as 640 × 400 dots or 640 × 350 dots, display control is performed so that the display area is always located at the center of the screen. Note that hatched portions in Figs. 7B and 7C represent non-display areas.

Fig. 8 is a detailed block diagram of the cathode timing generator 16.

In Fig. 8, a flip-flop (F/F) 21 outputs a generation timing signal 25 of the vertical shift clock (VSC) shown in Fig. 9D in accordance with the vertical sync signal (VSYNC) shown in Fig. 9B and the display period signal ($\overline{ENAB}$) shown in Fig. 9C. An AND gate 22 generates the vertical shift clock (VSC) shown in Fig. 9E in accordance with the signal 25 output from the F/F 21 and the horizontal sync signal (HSYNC) shown in Fig. 9A. A F/F 23 generates a timing signal 26 of the scanning data (SD) shown in Fig. 9F in accordance with the vertical sync signal (VSYNC) and the display period signal ($\overline{ENAB}$). A F/F 24 generates the scanning data (SD) shown in Fig. 9G in accordance with the signal 26 output from the F/F 23 and the vertical shift clock (VSC) output from the AND gate 22.

Note that the anode timing generator 12 has the same internal arrangement as that of the cathode timing generator 16 shown in Fig. 8, and can be realized by replacing the vertical sync signal (VSYNC) with the horizontal sync signal (HSYNC) and the horizontal sync signal (HSYNC) with the clock ($\overline{CLK}$) in Fig. 8.

Fig. 10 shows another embodiment of the cathode timing generator 16. In the embodiment shown in Fig. 8, the vertical shift clock (VSC) and the scanning data (SD) are generated using the display period signal ($\overline{ENAB}$). In the embodiment shown in Fig. 10, a vertical shift clock (VSC) shown in Fig. 11E and scanning data (SD) shown in Fig. 11F are generated in accordance with a vertical sync signal (VSYNC) shown in Fig. 11B and a horizontal sync signal (HSYNC) shown in Fig. 11A.

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In Fig. 10, a counter 31 generates a timing signal (Fig. 11C) for a display period in accordance with the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC). A F/F 32 extracts a timing signal of a first display period after generation of the vertical sync signal (VSYNC) from the signal 35 generated by the counter 31 and the vertical sync signal (VSYNC) so as to generate a timing signal 36 (Fig. 11D) for generating the vertical shift clock (VSC) and the scanning data (SD). An AND gate 33 generates the vertical shift clock (VSC) in accordance with the signal 36 generated by the F/F 32 and the horizontal sync signal (HSYNC). A F/F 34 generates the scanning data (SD) shown in Fig. 11F in accordance with the vertical shift block (VSC) generated by the F/F 32.

Figs. 12A through 12D are views for explaining a display position offset when no display period signal ($\overline{\text{ENAB}}$) is used. In Fig. 12A the horizontal sync signal (HSYNC) is normal, and in Fig. 12B the horizontal sync signal is shifted. Even if a display position is slightly offset on the screen of the CRT 5 due to the shifted horizontal sync signal (HSYNC) described above, display data is not partially omitted (Fig. 13D). However, on the PDP 4, even if the display position is offset slightly, display data is partially omitted (Fig. 13C). In contrast to this, when the display period signal ($\overline{\text{ENAB}}$) is used, the effective display period is designated, and the effective display data can be synchronized with the display timing. Therefore, as shown in Figs. 13E and 13F, the display position is not offset on the screen of the CRT 5, and data can always be displayed at a normal position.

Figs. 13A through 13F show differences in display position offset states between arrangements with and without using the display period signal ($\overline{\text{ENAB}}$). Fig. 13A shows a display state on the PDP 4 in a normal state, and Fig. 13B shows a display of the CRT 5 in a normal state, Fig. 13C shows a display state (a broken line portion indicates a portion corresponding to data omission) of the PDP 4 when a display position is offset due to the shifted horizontal sync signal (HSYNC) in an arrangement using no display period signal ($\overline{\text{ENAB}}$), and Fig. 13D shows a display state of the CRT 5 under similar conditions. Fig. 13E shows a display state (free from display data omission) of the PDP when the display position is offset due to the shifted horizontal sync signal (HSYNC) in an arrangement using the display period signal ($\overline{\text{ENAB}}$), and Fig. 13F shows a display state of the CRT under similar conditions.

The operations of the first and second embodiments of the present invention will now be described with reference to Figs. 1 through 13F.

The CRT controller 1 supplies the vertical sync signal (VSYNC), the horizontal sync signal (HSYNC), display data (DATA), and the like, which are the display timing signal of the CRT 5, to the PDP 4 and the CRT 5 through the driver 3. In this case, the polarities (positive/negative) of the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC) are changed in accordance with the display resolutions of the PDP 4 (640 × 480 dots/640 × 400 dots/640 × 350 dots) shown in Figs. 7A through 7C, as shown in Fig. 6. In other words, the CRT controller 1 is designed to change the polarities of the signals HSYNC and VSYNC in accordance with the display resolutions of the PDP 4. Furthermore, the CRT controller 1 supplies the display period signal ($\overline{\text{ENAB}}$) for designating the effective display period of the display data ($\overline{\text{DATA}}$) to the PDP 4 through the driver 3. The clock module 2 supplies the clock signal CLK to the PDP 4 through the driver 3.

The PDP 4 receives the various signals generated as the display timings of the CRT 5, and drives the display panel 19 in accordance with these signals.

The display data ($\overline{\text{DATA}}$) (4 bits/pixel; 16 gradation levels) is sent to the anode driver 18 through the data buffer 11 as the gradation data (GD).

The anode timing generator 12 receives the clock ($\overline{\text{CLK}}$), the display period signal ($\overline{\text{ENAB}}$), and the clock (MC) from the mode discrimination/clock generator 15, and generates the horizontal shift clock (HSC), the latch pulse (LP), and the like. The generator 12 outputs the generated signals to the anode driver 18.

The modulated pulse generator 13 generates the modulated pulse (MP) on the basis of the clock (MC) generated by the mode discrimination/clock generator 15, and outputs it to the anode driver 18. In this case, the pulse interval of the modulated pulse (MP) generated by the modulated pulse generator 13 can be used for uniform luminance adjustment over the entire gradation levels by the luminance adjustment variable resistor 14.

The mode discrimination/clock generator 15 discriminates the display resolution (Fig. 7) on the basis of the positive/negative polarities (Fig. 6) of the vertical sync signal (VSYNC) and the horizontal sync signal (VSYNC), and outputs the mode switching signal (MS). More specifically, when both the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC) have a negative polarity, the mode discrimination/clock generator 15 determines that the display resolution is 640 × 480 dots shown in Fig. 7B. When the vertical sync signal (VSYNC) has a positive polarity and the horizontal sync signal (HSYNC) has a negative polarity, the generator 15 determines that the display resolution is 640 × 400 dots shown in Fig. 7B. When the vertical sync signal (VSYNC) has a negative polar-

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ity and the horizontal sync signal (HSYNC) has a positive polarity, the generator 15 determines that the display resolution is 640 × 350 dots shown in Fig. 7C. The generator 15 supplies the mode switching signal (MS) to the cathode timing generator 16 together with the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC).

The cathode timing generator 16 receives the display period signal ($\overline{\text{ENAB}}$), the vertical sync signal (VSYNC), the horizontal sync signal (HSYNC), the mode switching signal (MS: 2 bits), which are output from the mode discrimination/clock generator 15, and generates signals, such as the scanning data (SD) (Figs. 4C and 5C), the vertical shift clock (VSC) (Figs. 4B and 5B), and the like, for driving the cathode electrodes of the display panel 19. The generator 16 supplies these signals to the cathode driver 17.

The cathode driver 17 receives the scanning data (SD) and the vertical shift clock (VSC) generated by the cathode timing generator 16, and outputs the cathode pulses (CAP0 through CAP479) (Figs. 4D through 4G and Figs. 5D through 5K) for driving the cathode electrodes.

Fig. 8 shows the internal arrangement of the cathode timing generator 16. Outputs Q of the F/Fs 21 and 23 go to low level, as shown in Figs. 9D and 9F, in response to the trailing edge of the signal VSYNC shown in Fig. 9B. An output Q of the F/F 21 is input to one input of the AND gate 22. As a result, during a low-level period of the Q output of the F/F 21, the signal VSC is not generated, as shown in Fig. 9E. The signal $\overline{\text{ENAB}}$ shown in Fig. 9C is applied to CLK input terminals of the F/Fs 21 and 23. For this reason, the Q output of the F/F 23 goes to high level at the trailing edge of the signal $\overline{\text{ENAB}}$, as shown in Fig. 9F, and the Q output of the F/F 21 goes to high level at the trailing edge of the signal $\overline{\text{ENAB}}$, as shown in Fig. 9D. Since the Q output (high level) of the F/F 23 is applied to the CLK terminal of the F/F 24, the F/F 24 raises the signal SD, as shown in Fig. 9G. Since the Q output of the F/F 21 is input to one input of the AND gate 22, the signal VSC is generated, as shown in Fig. 9E. Since the high-level signal VSC is supplied to a CLR terminal of the F/F 24, the signal SD goes to low level, as shown in Fig. 9G. In this manner, the vertical blanking period and the effective display period are distinguished by the signal $\overline{\text{ENAB}}$, and display data (scanning data) can be extracted.

On the other hand, the anode driver 18 receives the gradation data (GD) from the data buffer 11, the horizontal shift clock (HSC) and the latch pulse (LP) from the anode timing generator 12, and the modulated pulse (MP) from the modulated pulse generator 13, fetches the gradation data (GD) in its internal shift register in response to the horizontal shift clock (HSC), latches data of 640 pixels in its internal latch circuit in response to the latch pulse (LP), and performs pulse-width control in accordance with the modulated pulse (MP) so as to output the anode pulses (ANP0 through ANP639) each having a pulse width corresponding to gradation of pixel data.

The display panel 19 receives the cathode pulses (CAP0 through CAP479) output from the cathode driver 17 at the cathode electrodes, also receives the anode pulses (ANP0 through ANP639) at the anode electrodes, and outputs display data at a maximum display resolution of 640 × 480 dots (16 gradation levels).

Figs. 3A through 3J are timing charts showing timings of the various signals supplied to the PDP 4, and preset signal durations vary as shown in Fig. 6 in accordance with the corresponding display resolutions (640 × 480 dots/640 × 400 dots/640 × 350 dots).

Figs. 4A through 4R show signal states of the respective portions in the PDP 4 at the display resolution of 640 × 480 dots (Fig. 7A), and Figs. 5A through 5O show signal states of the respective portions in the PDP 4 at the display resolution of 640 × 400 dots (Fig. 7B) or 640 × 350 dots (Fig. 7C). Note that values in parentheses indicate those at the resolution of 640 × 350 dots. In Figs. 5A through 5O, the vertical shift clock (VSC) having a shorter interval than a display area is generated for upper and lower non-display areas (hatched portions shown in Figs. 7B and 7C) corresponding to 40 lines (or 65 lines) of the display screen, so that the operation timing of the display area is not suppressed. In this embodiment, each of the one-frame periods t1 of the display resolutions of 640 × 480 dots (Fig. 7B) and 640 × 350 dots (Fig. 7C) is shorter than the one-frame period t1 of the display resolution of 640 × 480 dots (Fig. 7A), as can be seen from Fig. 6. In this case, the one-frame period t1 at the display resolution of 640 × 480 dots corresponds to 60 frames per second, while the one-frame periods t1 at the display resolutions of 640 × 400 dots and 640 × 350 dots correspond to 70 frames per second each. This coincides with the display timing of the CRT 5.

The various constants shown in Fig. 6 are set so that a display area is always located at the center of the screen when the display resolution is lower than the physically maximum resolution on the display panel 19 like 640 × 400 dots or 640 × 350 dots.

Fig. 10 and Figs. 11A through 11F respectively show the arrangement of the cathode timing generator according to another embodiment of the present invention, and its timing charts.

In this embodiment, no display period signal is used, and the vertical shift clock (VSC) and the scanning data (SD) are generated on the basis of

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the vertical sync signal (VSYNC) and the horizontal sync signal (HSYNC).

More specifically, the signal VSYNC shown in Fig. 11B is supplied to CLR terminals of counters 31 and 32, and the signal HSYNC shown in Fig. 11A is supplied to a CLK terminal of the counter 31 and is also input to one input of an AND gate 33. As a result, as shown in Fig. 11C, the output from the counter 31 goes to low level at the trailing edge of the signal VSYNC, and the counter 31 counts the signal HSYNC. When the counter 31 counts a predetermined count (the period t3 (vertical back porch) shown in Fig. 6, i.e., 32H (1H = 32 msec) for 640 × 480 dots, 34H for 640 × 400 dots, and 59H for 640 × 350 dots), it supplies a carry signal to a CLK input terminal of the F/F 32. As a result, the Q output signal from the F/F 32 goes to low level at the trailing edge of the signal VSYNC, and goes to high level at the leading edge of the output from the counter 31, as shown in Fig. 11D. The high-level signal from the F/F 32 is supplied to the other input terminal of the AND gate 33 and a CLK input terminal of an F/F 34. As a result, as shown in Fig. 11F, the signal SD, the Q output of the F/F 34, goes to high level, the AND gate 33 outputs the signal VSC shown in Fig. 11E which is delayed by one period of the signal HSYNC, and the first clock of the signal VSC is supplied to the CLR terminal of the F/F 34. Therefore, the signal SD goes to low level, as shown in Fig. 11F. In this manner, the back porch period following the vertical sync signal is detected by the counter 31.

An offset of a display position when no display period signal ($\overline{\text{ENAB}}$) is used will be described below with reference to Figs. 12A through 12D and Figs. 13A through 13F. When the horizontal sync signal (HSYNC) is shifted from the normal state shown in Figs. 12A and 12B to a state shown in Figs. 12C and 12D, display data is not partially omitted even if a display position is slightly offset on the screen of the CRT 5 (Fig. 13D). However, display data is partially omitted even if the display position is slightly offset on the screen of the PDP 4 (Fig. 13C). In contrast to this, when the signal period signal ($\overline{\text{ENAB}}$) is used as in the embodiment described above, the effective display 3D), the display position is not offset on the screen of the PDP 4, and data can always be displayed at a normal position.

Claims

1. A plasma display control system having a CRT display controller (1), which comprises a plasma display and allows a CRT display to be connected thereto as an option, for outputting vertical and horizontal sync signals having polarities to said CRT display and said plasma display, characterized in that there are provided:
display resolution discriminating means (15) for discriminating the polarities of the vertical and horizontal sync signals output from said CRT controller, and determining selectable display resolution in accordance with the combination of polarities of the signals;
display timing generating means (12, 16) for generating a display timing signal in accordance with the selectable display resolution determined by said display resolution discriminating means; and
drive means (17, 18) for driving said plasma display responsive to the display timing signal generated by said display timing generating means.

2. A system according to claim 1, characterized in that said display resolution discriminating means, said display timing signal generating means, and said drive means are incorporated in said plasma display.

3. A system according to claim 1, characterized in that selectable display resolutions include 640 × 350 dots, 640 × 400 dots, and 640 × 480 dots.

4. A system according to claim 1, characterized in that said display timing signal generating means generates the display timing signal so that a display area is set at a central position of said plasma display when the display resolution is below a maximum display resolution of said plasma display.

5. A method of controlling a plasma display having a plurality of display resolutions and included in a CRT display controller which allows a CRT display to be connected thereto as an option, and outputs vertical and horizontal sync signals and data signals of data to be displayed on said CRT display and said plasma display, comprising:
discriminating the polarities of the vertical and horizontal sync signals output from said CRT controller, and determining a display resolution in accordance with the combination of the polarities of the signals;
generating a display timing signal in accordance with the determined display resolution; and
driving said plasma display in response to the generated display timing signal.

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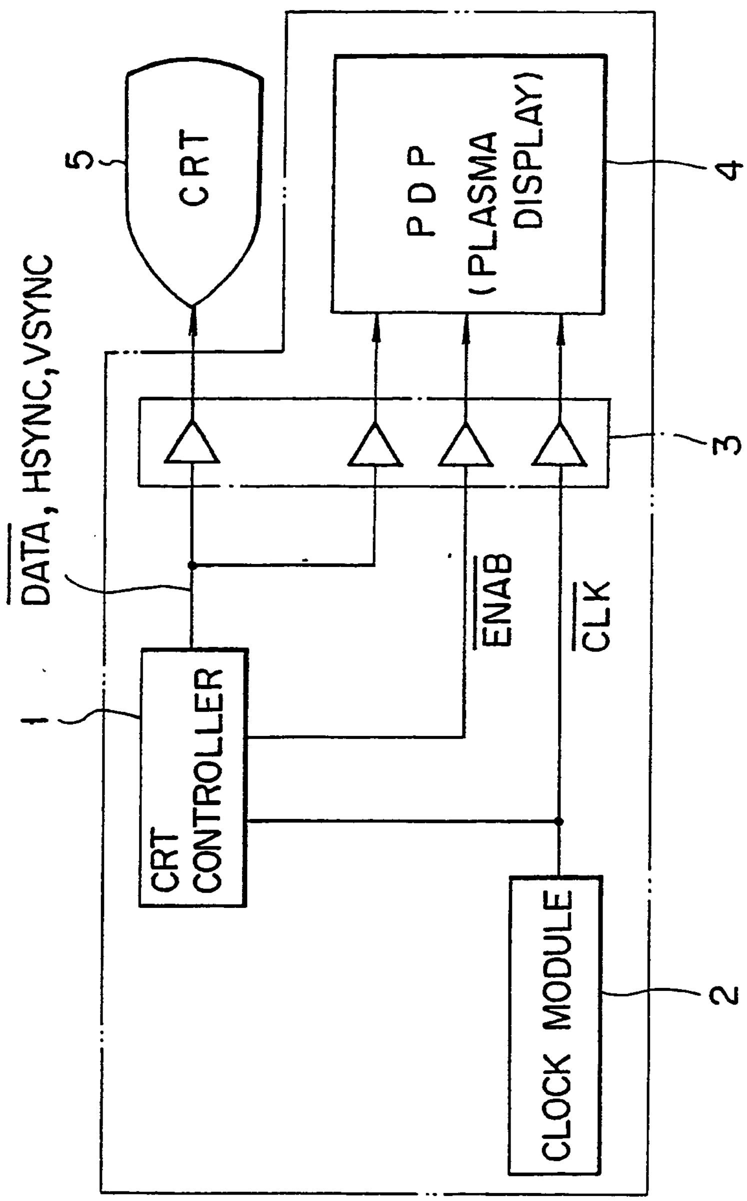

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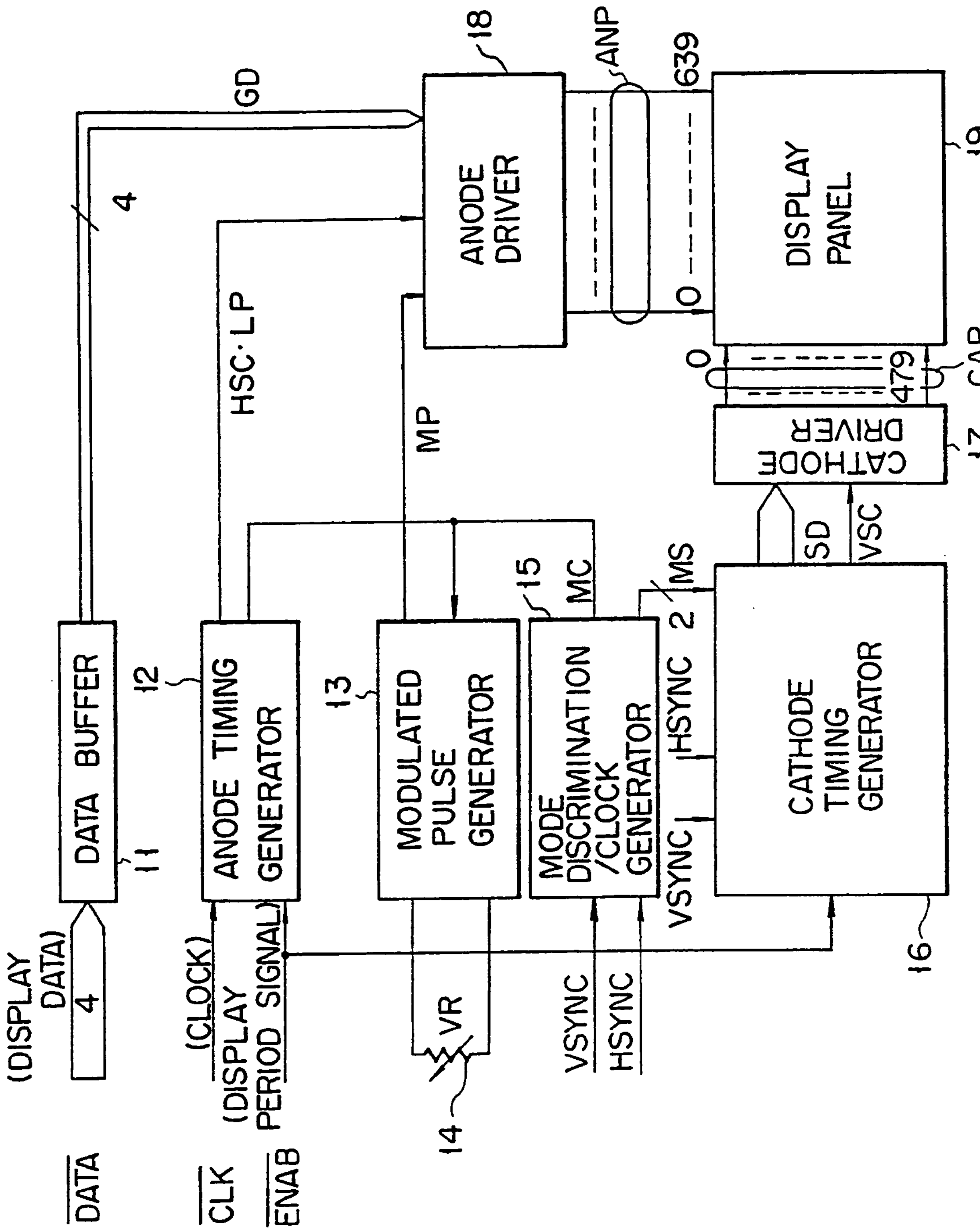

F I G. 2

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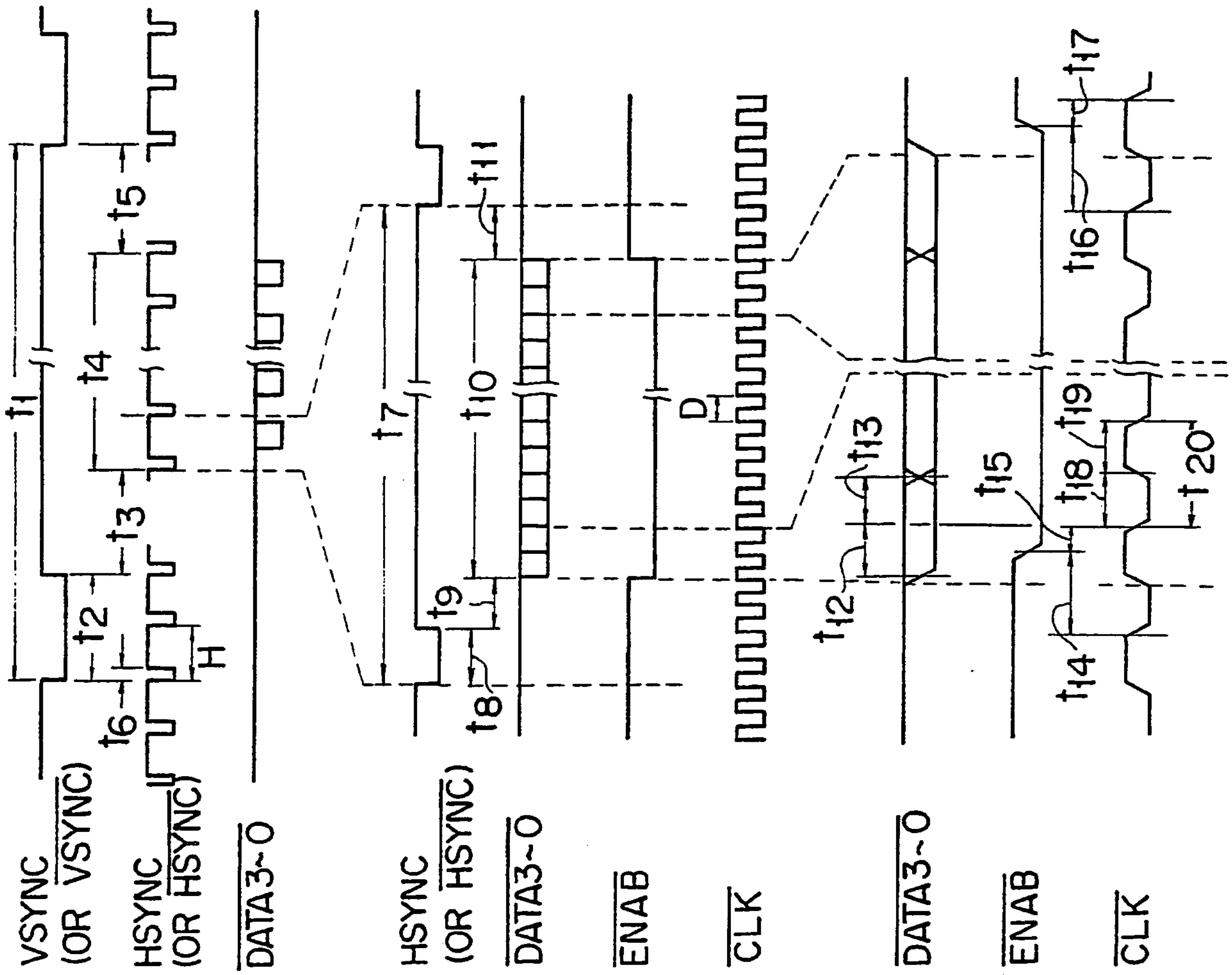


FIG. 3A
FIG. 3B
FIG. 3C
FIG. 3D
FIG. 3E
FIG. 3F
FIG. 3G
FIG. 3H
FIG. 3I
FIG. 3J

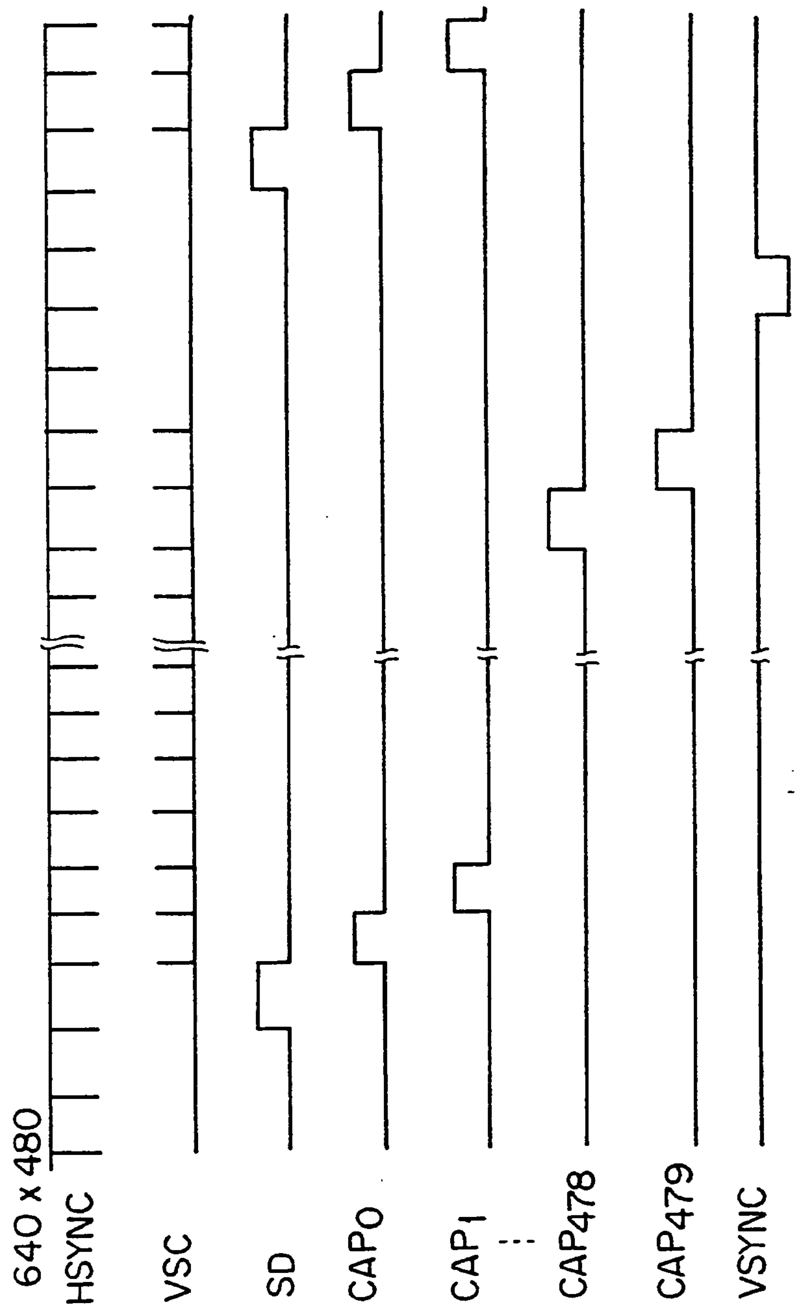
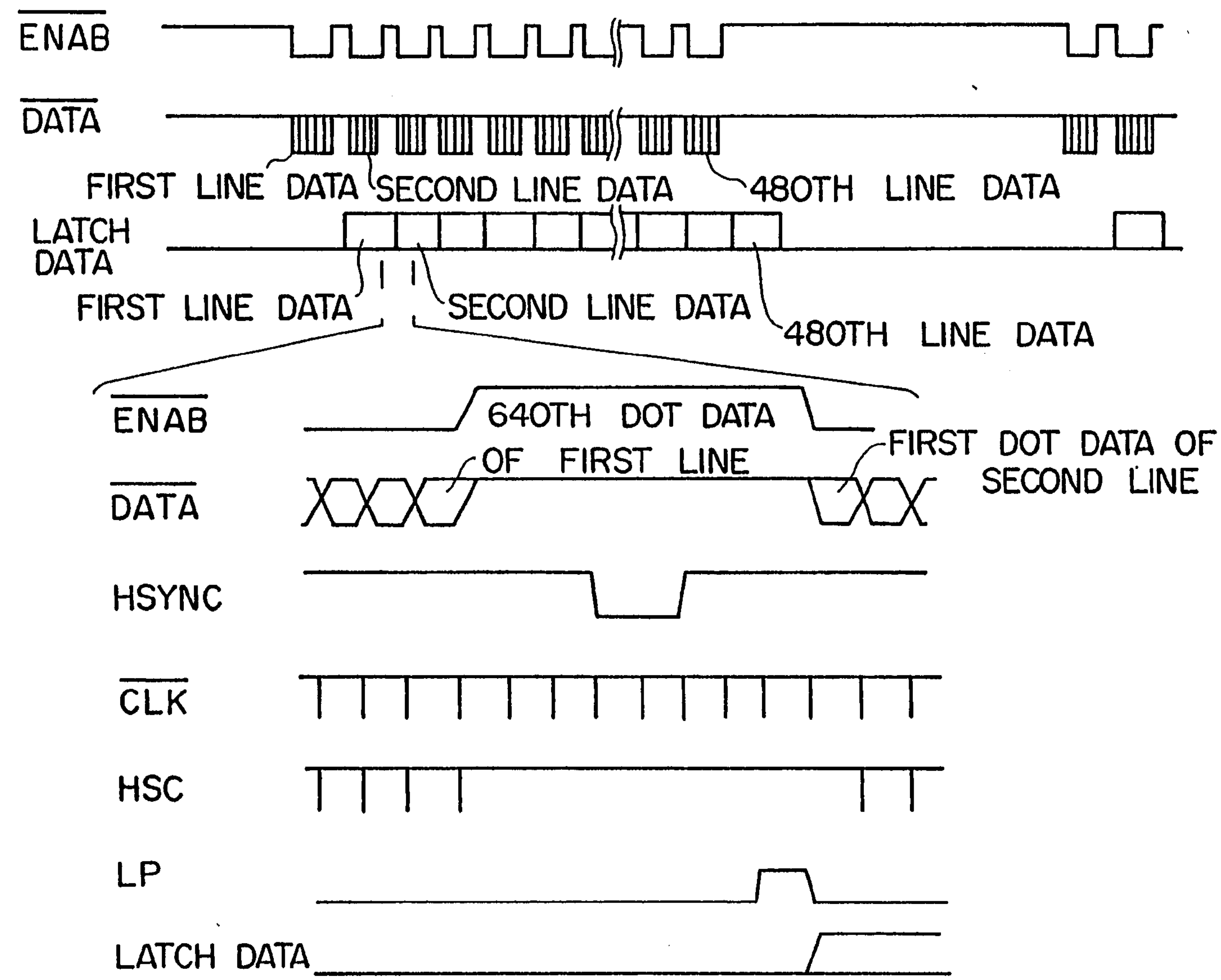


FIG. 4A
FIG. 4B
FIG. 4C
FIG. 4D
FIG. 4E
FIG. 4F
FIG. 4G
FIG. 4H

FIG. 4I
FIG. 4J
FIG. 4K
FIG. 4L
FIG. 4M
FIG. 4N
FIG. 4O
FIG. 4P
FIG. 4Q
FIG. 4R



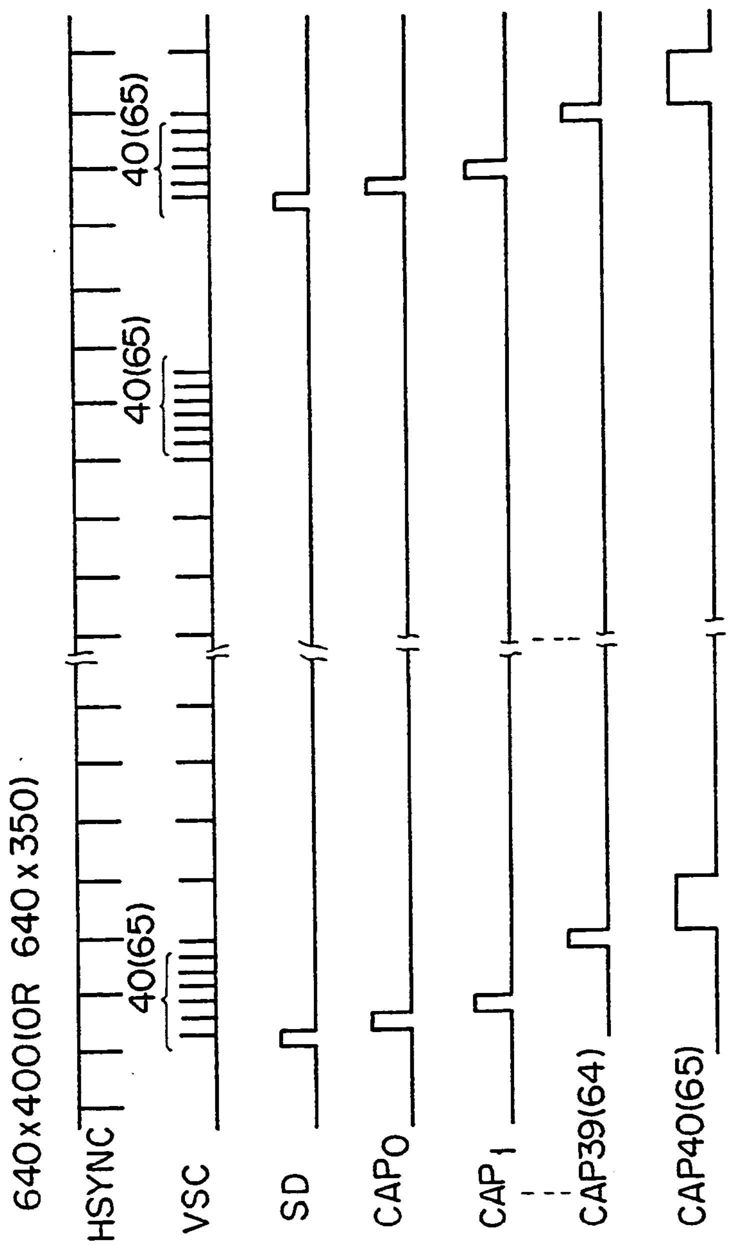


FIG. 5A
FIG. 5B
FIG. 5C
FIG. 5D
FIG. 5E
FIG. 5F
FIG. 5G

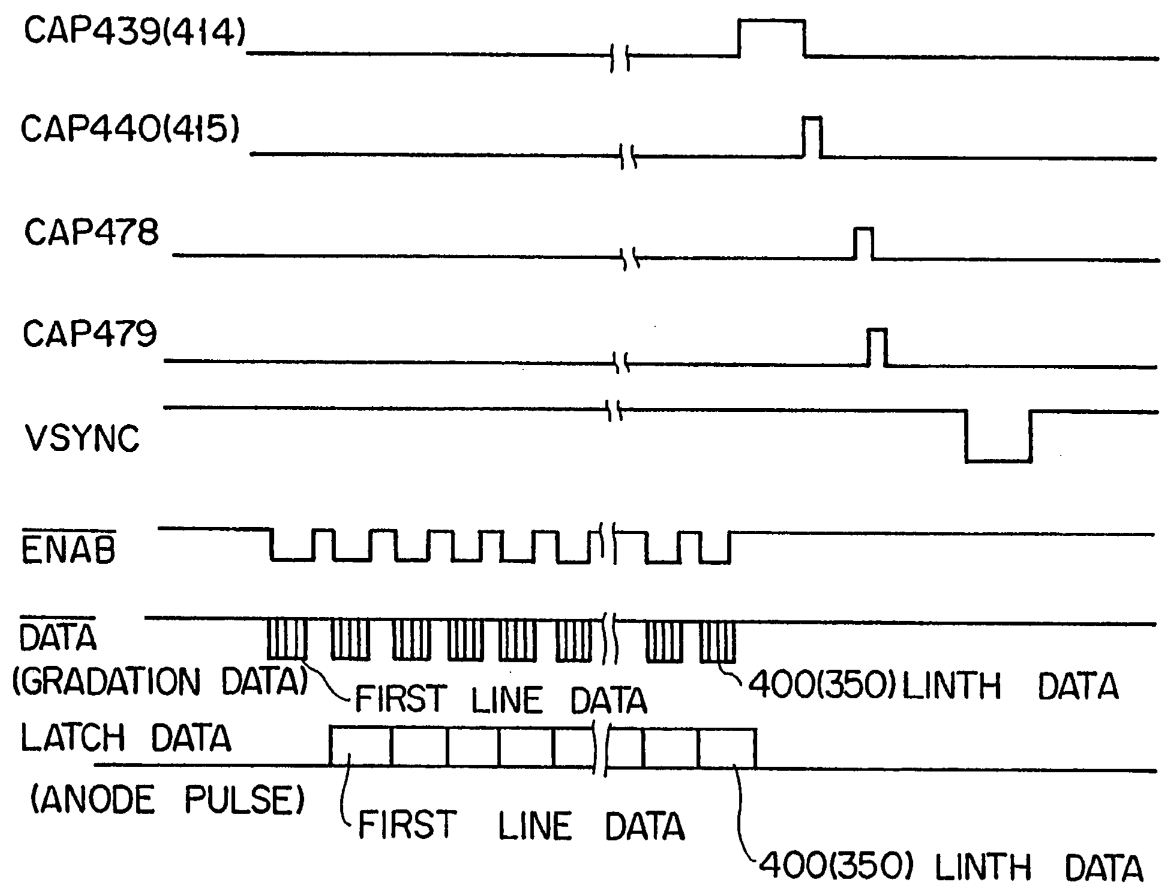
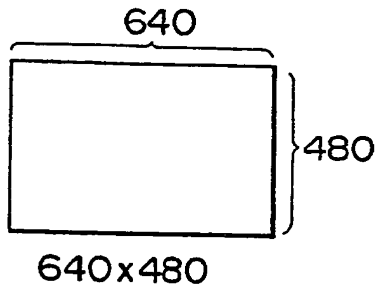


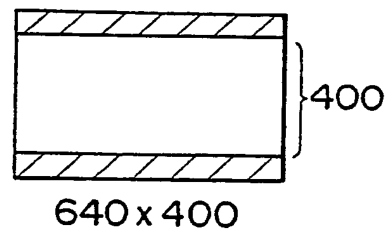
FIG. 5H
FIG. 5I
FIG. 5J
FIG. 5K
FIG. 5L
FIG. 5M
FIG. 5N
FIG. 5O

	640x480	640 x 400	640 x 350
VSYNC POLARITY	NEGATIVE	POSITIVE	NEGATIVE
HSYNC POLARITY	NEGATIVE	NEGATIVE	POSITIVE
t1	16.683ms(525H)	14.268ms(449H)	14.268ms(449H)
t2	0.064ms(2H)	0.064ms(2H)	0.064ms(2H)
t3	1.017ms(32H)	1.080ms(34H)	1.875ms(59H)
t4	15.253ms(480H)	12.711ms (400H)	11.122ms(350H)
t5	0.350ms(11H)	0.413ms(13H)	1.208ms(38H)
t6	3.813ms(96D)	3.813ms(96D)	3.813ms(96D)
t7 (=1H)	31.778ms(800D)	31.778ms(800D)	31.778ms(800D)
t8	3.813ms(96D)	3.813ms(96D)	3.813ms(96D)
t9	1.907ms(48D)	1.907ms(48D)	1.907ms(48D)
t10	25.422ms(640D)	25.422ms(640D)	25.422ms(640D)
t11	0.636ms(16D)	0.636ms(16D)	0.636ms(16D)

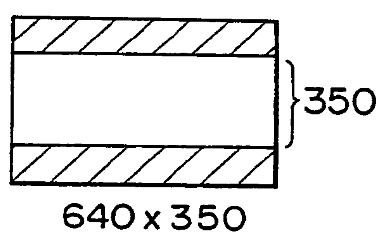
F I G. 6



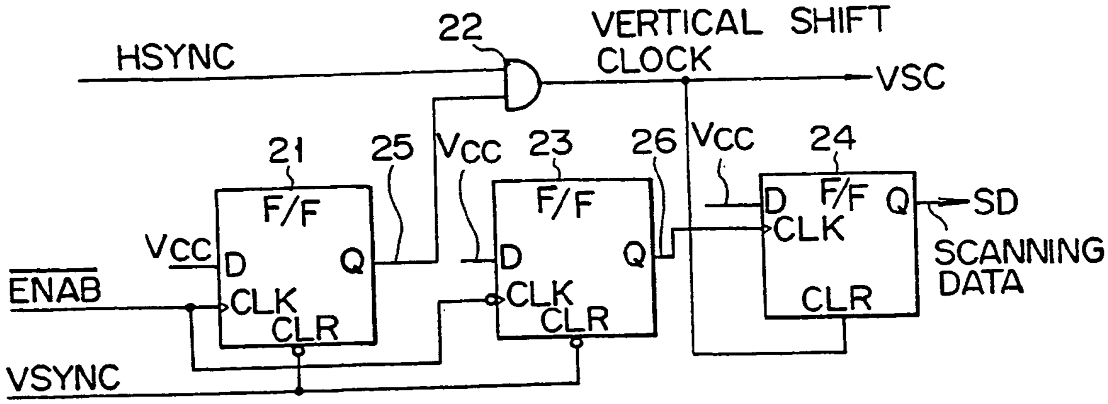
F I G. 7A



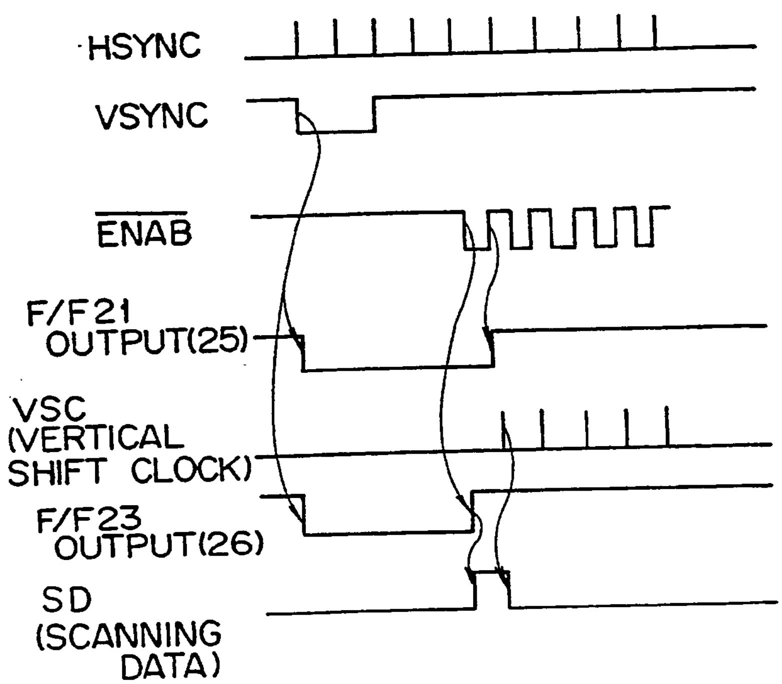
F I G. 7B



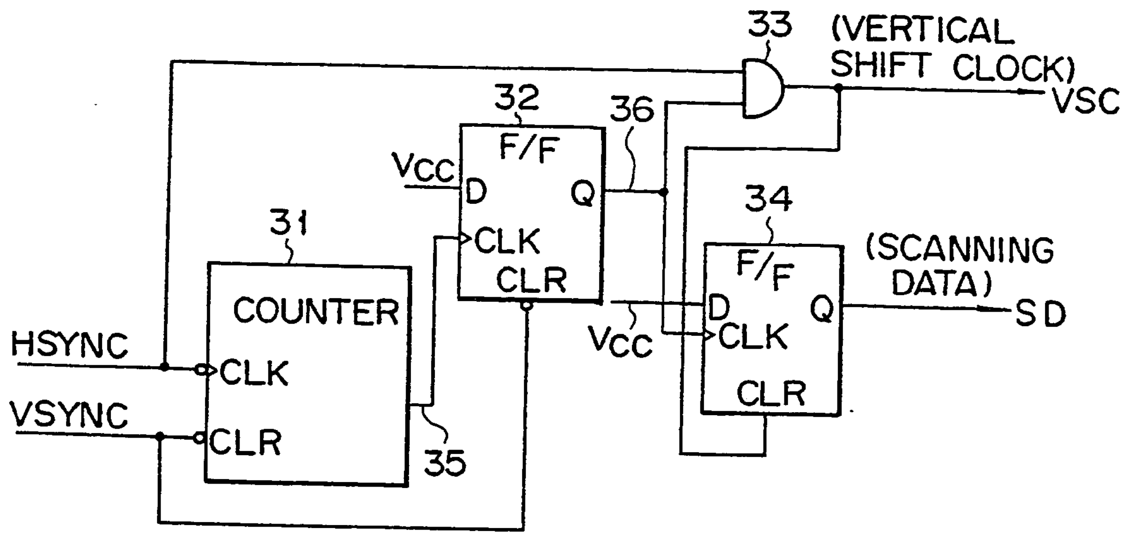
F I G. 7C



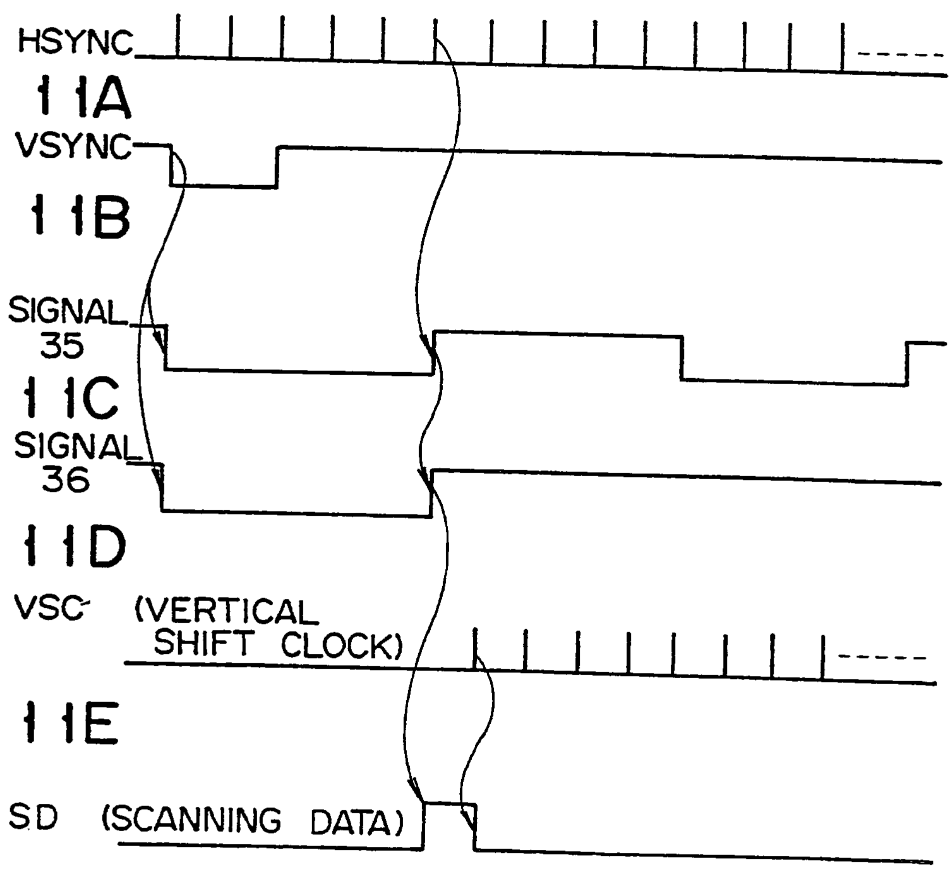
F I G. 8



F I G. 9A
F I G. 9B
F I G. 9C
F I G. 9D
F I G. 9E
F I G. 9F
F I G. 9G



F I G. 10



F I G. 11A

F I G. 11B

F I G. 11C

F I G. 11D

F I G. 11E

F I G. 11F

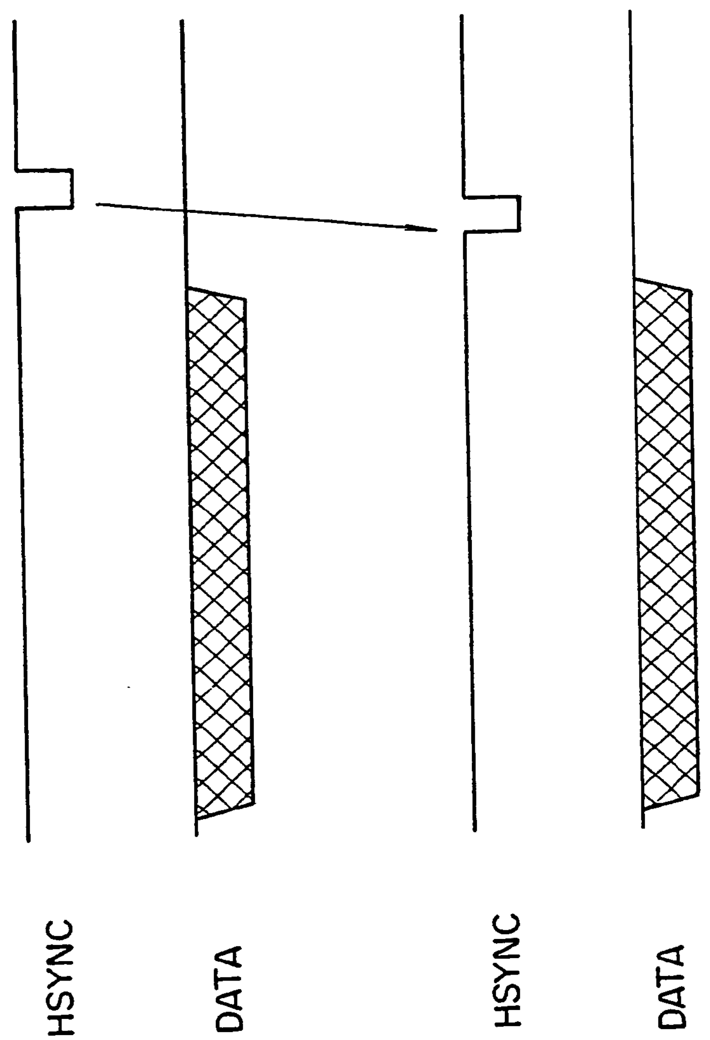


FIG. 12A

FIG. 12B

FIG. 12C

FIG. 12D

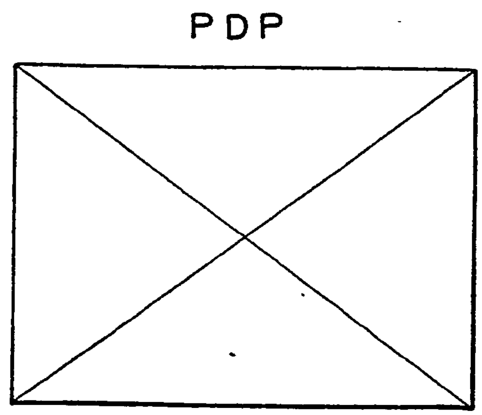


FIG. 13A

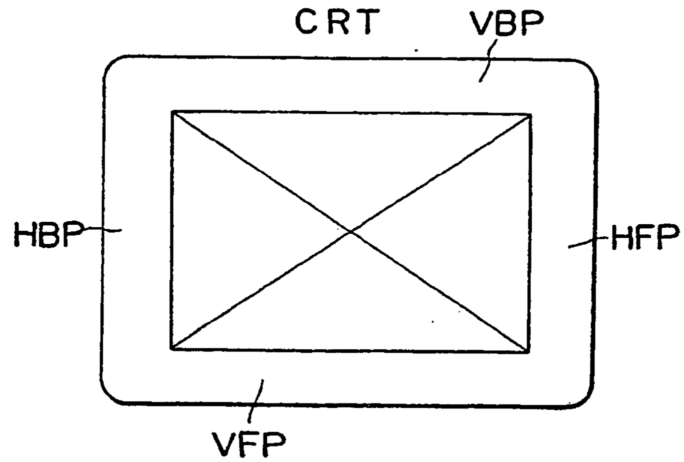


FIG. 13B

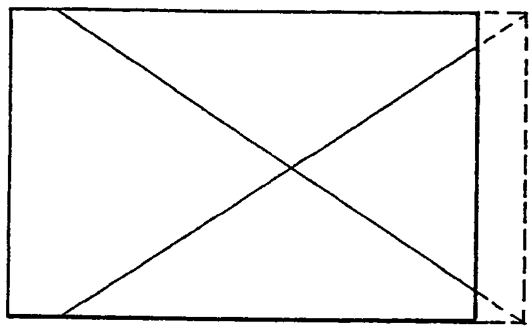


FIG. 13C

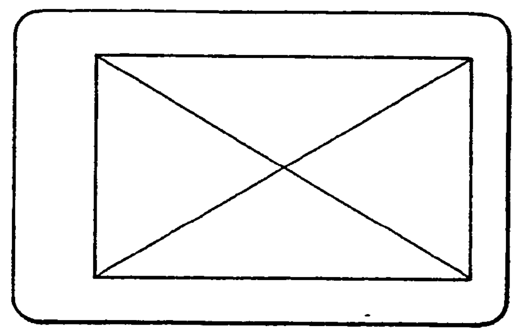


FIG. 13D

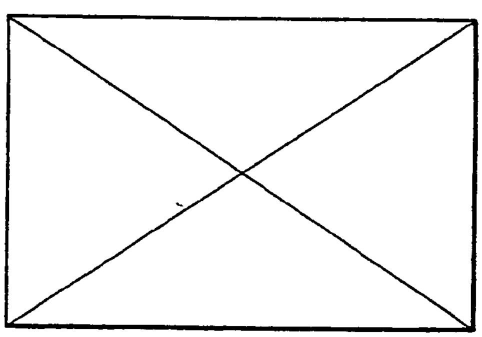


FIG. 13E

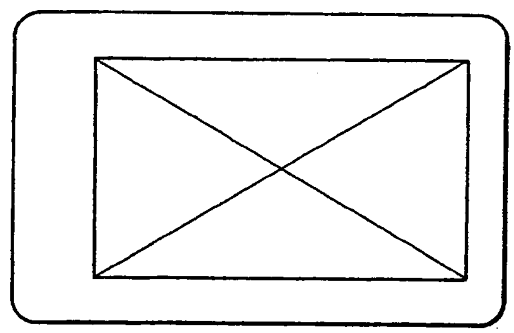


FIG. 13F

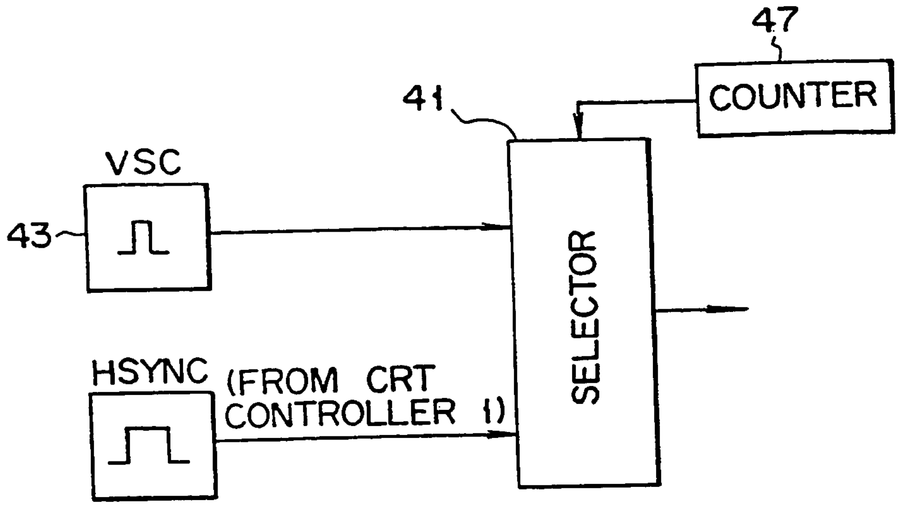


FIG. 14

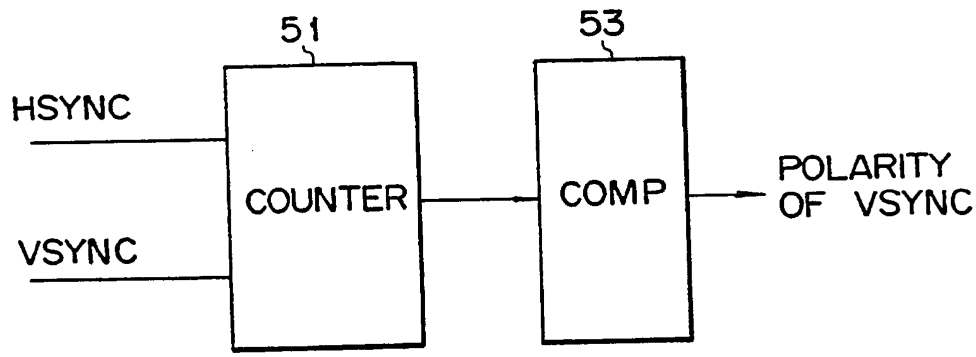


FIG. 15

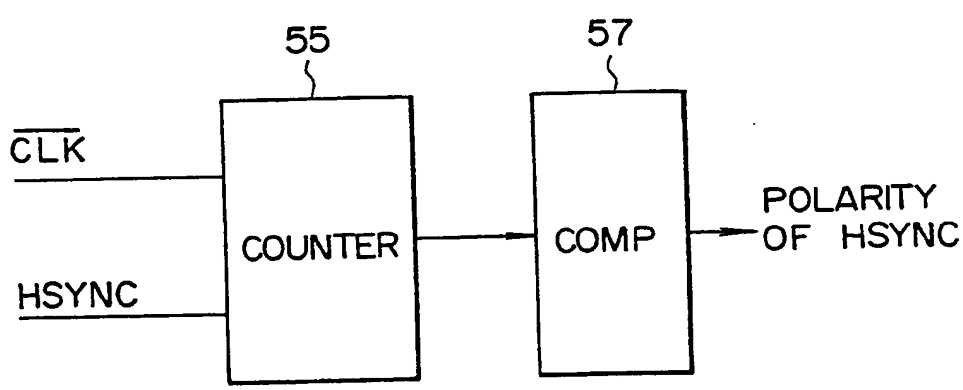


FIG. 16

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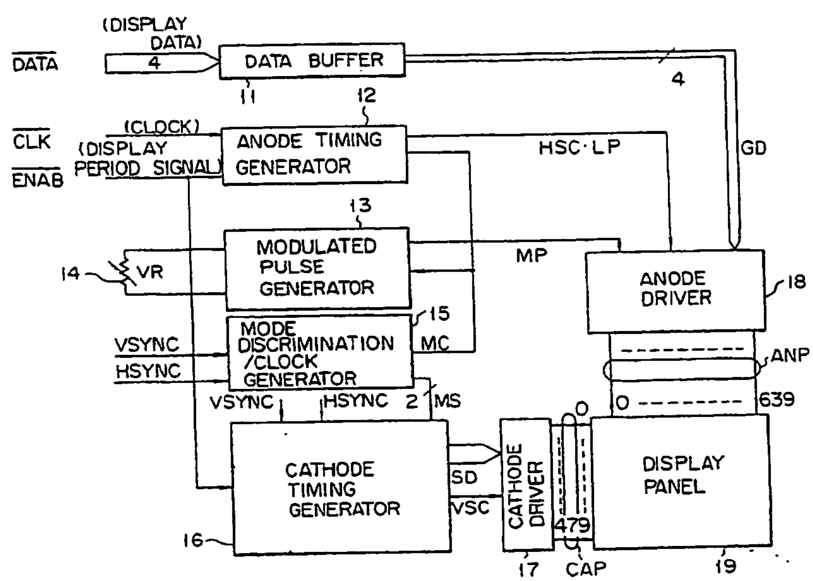
(54) **Plasma display control system.**

(57) A plasma display includes a mode discrimination/clock generator (15). A CRT display controller (1) generates vertical and horizontal sync signals having polarities. The mode discrimination/clock generator (15) discriminates the polarities of the vertical and horizontal sync signals to determine a display resolution. Anode and cathode timing generators (12, 16) generate display timing signals in accordance with the display resolution.



F I G. 2

EP 0 344 621 A3

European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 10 9478

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 611 203 (T.N. CRISCIMAGNA et al.) * Figures 1,4; abstract; column 2, lines 28-55 * – – –	1,5	G 06 F 3/14 G 09 G 3/28
A	EP-A-0 195 203 (ASCII CO.) * Figure 6; abstract; claim 1 * – – –	1,5	
A	US-A-4 684 936 (BROWN et al.) * Figure 2; abstract; column 3, lines 5-37; column 5, lines 24-51 * – – – – –	1,5	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 06 F
G 09 G

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	25 April 91	CORSI F.

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X: particularly relevant if taken alone
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